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Amendments to the Specification:

Please replace paragraph beginning on page 16, line 20 with the following amended paragraph:

Attention is here directed to FIG. 3, which constitutes a timing diagram that articulates the temporal relationships between significant signals introduced above, as these signals may arise in accordance with one embodiment of the invention. As may be seen in FIG. 3, the set of time-variant and interrelated signals defined therein include the RECADDR 31, system clock (CLK) 32, ADV 33, PFADDR 34, PFDONE 35, PWRDN 36, PFHIT 37, ADDROUT 38 (at ADDROUT output 236 of MUX 23 in FIG. 2), and DATA OUT 39. Initially, at time 311 a received address, REC0 appears from, for example, a system processor. Reception of the address REC0 is coincident with the rising edge of CLK 32 that appears at time 321, as well as with the falling edge of ADV that occurs at time 331. Because the address received at the time 311 is, for purposes relevant here, assumed to be the initial received address, output 136 of MUX 13, ADDROUT, will assume a value of ADRO0 at time 381, also coincident with times 311, 321 and 331. Assuming, for pedagogical purposes, that the memory read latency is six CLK periods, then corresponding data will appear at the memory output at time 391, six CLK cycles after the reception of the initial received address at time 311. At time 341, the RSM prefetch address generator outputs the first prefetched address PF1, resulting in a PFDONE pulse that has a rising edge at time 351. Similar rising edges occur at times 352 and 353. The next corresponding received address, REC1, appears at time 312, after which the falling edge of ADV occurs at the time [[322]] 332. Note that similar falling edges occur at times 333 and 334. Because, according to FIG. 3, the received address represents at hit, PFHIT assumes a logic level ONE at time 371. Consequently, output 236 of MUX 13 selects the prefetched address, and PFADDR is coupled to the memory device. Corresponding DATAOUT appears at time 392. The next address cycle similarly results in a hit, and at time 384 the prefetched address, PF2, that is available at time 342 appears as ADDROUT. Corresponding data arrives at time 393. PFHIT persists at a logic level ONE. Note the various values of ADDROUT at times 382, 383, and 385.

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